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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

A pipeline analog-to-digital converter with correction of inter-stage gain errors

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The present invention relates to an Analog-To-Digital converter with a pipeline architecture.

Analog-To-Digital (ADC) converters are commonly used in a wide variety of applications (for example, in the telecommunication field), whenever an analog signal is to be converted into a corresponding digital signal. For this purpose, many kinds of converters have been proposed in the last years. In a particular architecture, known as pipeline or multistage, the converter uses a series of stages providing successive approximations of the digital signal.

Particularly, each stage performs a low-resolution conversion and produces a sub-set of the desired bits of the digital signal. A residue of the analog signal (representing a quantization error of the conversion) is then passed to a next stage in the pipeline; the next stage generates a further sub-set of lower significant bits of the digital signal, and so on until the last stage of the pipeline. This architecture provides high resolutions, using very simple and inexpensive stages.

Typically, the residues are amplified by a pre-set analog gain before being passed to the next stages; in this way, each stage operates with a similar input signal range. However, any error in the (inter-stage) gain causes a harmonic distortion in the digital signal generated by the converter.

This problem is particular acute in the first stages of the pipeline (since the corresponding error in the inter-stage gain is amplified by all the next stages). The inherent imprecision of the inter-stage gain (due to the limits of the technological process used to implement the converter) then strongly reduces the actual resolution that

can be achieved.

For example, a converter at 14 bits with stages at 1 bit (wherein the inter-stage gain is 2), would require a precision in the inter-stage gain of the first stage equal to $1/2^{13} \simeq 0.012\%$; this precision is substantially impossible to achieve, particularly when the converter is integrated in a chip of semiconductor material (or in any case it would require very expensive manufacturing techniques, such as laser trimming processes).

It is an object of the present invention to overcome the above-mentioned drawbacks. In order to achieve this object, a converter as set out in the first claim is proposed.

Briefly, the present invention provides an analog-to-digital converter with a pipeline architecture for converting an analog input signal into a digital output signal with a predefined resolution, wherein the converter includes a plurality of stages each one having means for converting an analog local signal into a digital local signal with a local resolution lower than said resolution, means for determining an analog residue indicative of a quantization error of the means for converting, and means for amplifying the analog residue by an inter-stage gain corresponding to the local resolution to generate the analog local signal for a next stage, and wherein the converter further includes means for combining the digital local signals of all the stages into the digital output signal weighting each digital local signal according to a digital weight depending on the corresponding inter-stage gain; the means for combining includes, for at least one of the stages, means for dynamically estimating a digital

correction signal indicative of an analog error of the corresponding inter-stage gain, and means for controlling the digital weight according to the digital correction signal.

Moreover, a corresponding analog-to-digital conversion method is also encompassed.

Further features and the advantages of the solution according to the present invention will be made clear by the following description of a preferred embodiment thereof, given purely by way of a non-restrictive indication, with reference to the attached figures, in which:

Figure 1 is a schematic block diagram of a converter known in the art;

Figure 2 shows a preferred embodiment of the converter according to the present invention; and

Figure 3 depicts the functional blocks of a logic module of the converter of the invention.

With reference in particular to Figure 1, an Analog-To-Digital (ADC) converter 100 is shown; the converter 100 receives a (continuos) wide-band analog input signal IN, which is converted into a corresponding digital output signal OUT (for example, with a resolution of 16 bits). The converter 100 has a pipeline architecture with multiple cascade-connected stages 105_3-105_0 (four in the example at issue). Each stage 105_3-105_0 performs a low-resolution conversion (for example, generating B=4 bits of the digital output signal OUT), and provides an analog signal, indicative of a quantization error of the conversion, to the next stage.

In detail, as shown in the expanded view of a generic stage (for example, the first stage 105_3), a sample/hold

(S/H) amplifier 110 receives an analog (local) input signal Vin from the previous stage (with Vin=IN for the first stage 105_3). The sampled signal Vin is supplied to a flash ADC 115, so as to be converted into a corresponding digital (local) output signal Dout of B=4 bits; the digital output signal Dout represents the analog input signal Vin with the addition of a residue eq introduced by the quantization error of the ADC 115 (in the following, the analog signals and the corresponding digital signals will be denoted with the same symbols for the sake of simplicity).

The digital output signal Dout is also applied to a Digital-To-Analog (DAC) converter 120. The DAC 120 re-converts the digital output signal Dout into a corresponding analog signal. An adder 125 subtracts the analog output signal Dout=Vin+eq from the analog input signal Vin (from the sample/hold amplifier 110). The resulting analog residue (-eq) is applied to an amplifier 130 having an analog inter-stage gain 2^B. The amplifier 130 generates an analog output signal Vout=(-eq)2^B that is passed to the next stage (with the exception of the last stage 105_0 containing the ADC 115 only). In this way, the next stage operates with a similar input signal range (being the dynamic of the analog residue eq equal to Vin/2^B).

A shifter 135 combines the signals Dout provided by all the stages 105_3-105_0 into the overall digital output signal OUT. Particularly, the last stage 105_0 directly generates the 4 least significant bits (LSB) of the digital output signal OUT. The last but one stage 105_1 provides the 4 more significant bits of the digital output signal OUT; as a consequence, the digital signal Dout output by the stage 105_1 is multiplied by a digital weight 2^B corresponding to

the inter-stage gain (i.e., it is shifted of B positions) and then added to the digital signal Dout output by the stage 105_0. Likewise, the digital signal Dout output by the stage 105_2 is weighted by a factor $2^B2^B=2^{2B}$ (i.e., it is shifted of 2B positions), and so on until the first stage 105_3 that provides the 4 most significant bits (MSB) of the digital output signal OUT.

Considering now Figure 2, a pipeline converter 200 according to a preferred embodiment of the present invention is shown (the elements corresponding to the ones shown in Figure 1 are denoted with the same references, and their explanation is omitted for the sake of simplicity). In the figure, all the signals placed above the horizontal dotted line are analog, whereas all the signals placed below this line are digital.

The invention is based on the intuition that the desired resolution of the converter can be achieved even irrespectively of the precision of the amplifiers providing the inter-stage gains. In the proposed algorithm, the analog error introduced by each amplifier is estimated dynamically; the digital output signals are then combined weighting them according to digital factors that approximate the inter-stage gains with the desired precision.

In the example shown in the figure, the concepts of the present inventions are applied to the first stage 115_3 of the converter only. In this case, the stage 115_3 passes the analog output signal Vout (indicative of the corresponding quantization error) to the next stages of the pipeline (denoted as a whole with 105_{20}). A shifter 203 (corresponding to a portion of the circuit 135 of Figure 1) combines the digital signals output by the stages 105_{20} as

in the prior art. A new circuit 204 then combines (according to the proposed algorithm) the digital signal output by the stage 105_3 with the result of the conversion performed by the next stage 105_{20} (from the shifter 203).

In detail, a Pseudo-Random Noise (PRN) generator 205 provides a digital test signal t of 1 bit; the digital test signal t takes the logic values 0,1 with a law that simulates randomness. A DAC 210 converts the digital test signal t into a corresponding analog signal. An adder 215 sums the analog test signal t to the analog input signal Vin (from the sample/hold amplifier 110). The resulting analog signal Vin+t is applied to the ADC 115, so as to be converted into a corresponding digital signal Vin+eq+t (wherein eq is the residue introduced by the quantization error of the ADC 115). In order to avoid overflow of the ADC 115 (when the analog input signal Vin reaches its full-scale value), the dynamic of the analog test signal t should be lower than a half LSB of the ADC 115 (for example, -10mV for the logic value 0 and +10mV for the logic value 1).

As a consequence, the amplifier 130 receives an analog signal -eq-t from the adder 125. Denoting with e the (unknown) analog error of the amplifier 130, the analog output signal Vout that is passed to the next stages 105_{20} will be $(-eq-t)2^B(1+e)$. The next stages 105_{20} convert this analog signal into corresponding digital output signals; the shifter 203 accordingly combines these digital output signals into a digital signal $(-eq-t)G(1+e)$, wherein G is the digital representation of the (ideal) total inter-stage gain of the stages 105_3-105_1.

At the same time, a multiplier 220 multiplies the digital signal Vin+eq+t (from the ADC 115) by the digital

weight G, so as to output a digital signal (Vin+eq+t)G. A further multiplier 225 performs the same operation. The resulting digital signal (Vin+eq+t)G is then applied to an input of a multiplier 230; the other input of the multiplier 230 receives a digital correction signal ê (generated as described in the following); as a consequence, the multiplier 230 outputs a digital signal (Vin+eq+t)Gê.

The digital signal (-eq-t)G(1+e) from the shifter 203, the digital signal (Vin+eq+t)G from the multiplier 220, and the digital signal (Vin+eq+t)Gê from the multiplier 230 are provided to an adder 235. The resulting digital signal Vin(1+ê)G+(eq+t)G(ê-e) is input to a logic module 240. The logic module 240 also receives the digital test signal t from the PRN generator 205 directly. The logic module 240 estimates the digital correction signal ê correlating these input signals; particularly, the logic module 240 calculates the digital correction signal ê that approximates the digital representation of the analog error e minimizing their difference according to a Least Mean Square Algorithm (LMS).

The digital signal Vin(1+ê)G+(eq+t)G(ê-e) from the adder 235 represents the digital output signal OUT of the whole converter 200. In the ideal condition wherein ê=e, the digital output signal OUT is then equal to Vin(1+ê)G. In this way, the additive term (including the digital test signal t) due to the analog error e of the amplifier 130 providing the inter-stage gain is deleted; therefore, the harmonic distortion caused by the imprecision of the inter-stage gain is eliminated, or at least substantially reduced (the remaining term (1+ê) is a simple scaling factor, which does not affect the digital output signal OUT).

Experimental results have shown that the structure described above provides higher performance (measured by the Equivalent Number Of Bits, or ENOB, parameter); for example, a converter at 14 bits with an analog error equal to 2% in the inter-stage gain, nevertheless exhibits a Signal to Noise Distortion Ratio (SNDR) and a Spurious Free Dynamic Range (SFDR) that are close to their theoretical values.

However, the concepts of the present invention are also applicable when the analog input signal is of a different type, when the pipeline converter includes another number of stages, or when each stage provides a different number of bits (down to a single one). Similar considerations apply if the test signal has a different dynamic, or if equivalent functional blocks are used. Moreover, although the pipeline converter has been described with a simplified combination of the digital signals output by the different stages, similar considerations apply if these digital signals are combined in a different manner; for example, the range of each stage is typically greater than one LSB of the previous stage (for digital error correction). Likewise, the same concepts are applicable to the next stages of the pipeline; in this case, the digital signal output by each one of the involved stages is weighted according to a digital correction signal that estimates the analog error in the inter-stage gain of both the current stage and the next (involved) stages.

Moving now to Figure 3, the logic module 240 includes a multiplier 305 receiving the digital signal $Vin(1+\hat{e})G+(eq+t)G(\hat{e}-e)$ and the digital test signal t. The digital signal resulting from their product, i.e. $tVin(1+\hat{e})G+t(eq+t)G(\hat{e}-e)$, is applied to a sinc filter 310 of

the first order. The sinc filter 310 calculates the mean value of a number of samples of the input signal defined by a decimation parameter (for example, 1024). In this way, the multiplier 305 and the sinc filter 310 perform an operation that approximates a correlation of the digital signal $Vin(1+\hat{e})G+(eq+t)G(\hat{e}-e)$ and of the digital test signal t. The result of this operation provides a digital signal, which is proportional to a residual difference of the digital correction signal $\hat{e}$ with respect to the digital representation of the analog error e (being the signals Vin and t non-correlated to each other, so that the term $tVin(1+\hat{e})G$ disappears in the mean value).

A multiplier 315 scales down the digital residual difference by a digital weight μ stored in a register 320. The resulting digital signal is provided to an integrator, which calculates the digital correction signal $\hat{e}$. In detail, a delay block 325 (implemented with a bank of flip-flops) accumulates the digital correction signal $\hat{e}$. An adder 330 sums the (scaled-down) digital residual difference to the (previous) digital correction signal $\hat{e}$, which is provided by the delay block 325 with a feedback loop. The resulting (current) digital correction signal $\hat{e}$ is then latched by the delay block 325. In this way, the digital correction signal $\hat{e}$ converges towards the digital representation of the analog error e (until their difference falls below a threshold value).

The digital weight μ defines the precision and the convergence speed of the process. Low values of the digital weight μ increase the precision; in this case, the digital residual difference affects the digital signal applied to the integrator 325,330 to a lower extent, so as to

compensate for the inherent imprecision of the sinc filter 310 (caused by the finite number of samples taken into consideration); however, this slows down the convergence speed of the process. Conversely, high values of the digital weight μ increase the convergence speed of the process, but reduce its precision. The process can be controlled also acting on the decimation parameter of the sinc filter 310. In fact, a higher number of samples increases the precision of the correlation and then of the whole process.

However, the concepts of the present invention are also applicable when the logic module has a different structure or includes equivalent functional blocks; for example, similar considerations apply if the sinc filter is replaced with an equivalent element, if the decimation parameter has another value, if the digital residual difference is scaled down in a different manner, and the like.

More generally, the present invention proposes an analog-to-digital converter with a pipeline architecture, which is used to convert an analog input signal into a digital output signal with a predefined resolution. The converter includes a plurality of stages. Each stage has means for converting an analog local signal into a digital local signal with a local resolution (which is lower than said resolution). Means are provided for determining an analog residue indicative of a quantization error of the means for converting. The stage also has means for amplifying the analog residue by an inter-stage gain corresponding to the local resolution, in order to generate the analog local signal for a next stage. Moreover, the converter further includes means for combining the digital local signals of all the stages into the digital output

signal; this result is achieved weighting each digital local signal according to a digital weight depending on the corresponding analog gain. In the converter of the invention the means for combining includes, for one or more of the stages, means for dynamically estimating a digital error indicative of an analog error of the corresponding analog gain; means are then used for controlling the digital weight according to the digital error.

The solution of the invention substantially reduces the distortion (in the digital signal generated by the converter) caused by the analog error in the inter-stage gain.

This result is achieved operating in the digital domain; moreover, it is independent of the precision of the analog amplifier providing the inter-stage gain.

Therefore, the proposed solution virtually makes it possible to obtain any desired resolution of the converter. In any case, the design specifics of the analog components included in the converter can be relaxed. This results in a reduction of the power consumption and of the occupied area (when the converter is integrated in a chip of semiconductor material); moreover, the converter can be manufactured at lower cost (for the same precision).

The above describe advantages are particularly important when the converter works with a wide-band analog input signal; moreover, these advantages are clearly perceived if the converter is used in consumer products, especially if they are portable (such as mobile telephones); however, different applications of the converter are contemplated and within the scope of the present invention.

The preferred embodiment of the invention described

above offers further advantages.

Particularly, the digital correction signal is estimated exploiting a digital test signal that is input into the stage (and then comparing the digital test signal with the digital local signals of the next stages in the pipeline).

The proposed technique can be used in the background, without interfering with operation of the converter.

Preferably, the digital correction signal is obtained correlating the digital test signal with the digital local signals of the next stages (assuming that the digital test signal and the analog input signal are non-correlated).

This solution provides a very high degree of accuracy.

A suggested choice for the digital test signal is that of a pseudo-random signal.

In this way, inexpensive components can be used to generate a digital test signal that is always non-correlated with the analog input signal.

Advantageously, the digital test signal is converted into a corresponding analog test signal and then added to the analog local signal.

The proposed structure makes it possible to achieve the desired result without any risk of overflow.

However, the solution according to the present invention leads itself to be implemented even exploiting different techniques for dynamically estimating the digital correction signal. Alternatively, the test signal is generated in a different manner or is inserted in another position (provided that its transfer function is the same as the one of the analog residue).

In a preferred embodiment of the present invention, the

correlation is performed suitably weighting and summing the digital signal output by the stage with the digital signal provided by the next stages in the pipeline.

These operations are used to remove (in a very simple manner) both the effects of the analog error in the inter-stage gain and the digital test signal from the result of the whole conversion.

As a further enhancement, a digital residual difference of the correlation process is scaled down.

This additional feature makes it possible to tune the process according to the opposed requirements of precision and speed.

A suggested choice for implementing the correlation process is that of using a sinc filter.

The proposed scheme provides an additional way of controlling the precision of the process (acting on the decimation parameter of the sinc filter); for example, the digital residual difference can be scaled down to a lower extent (thereby increasing the speed of the process) when a higher decimation parameter is used.

Preferably, the concepts of the present invention are applied to one or more of the first stages in the pipeline.

In this way, the analog errors in the inter-stage gains are corrected only when they are more deleterious.

However, the converter according to the present invention is also suitable to be implemented performing the correlation in a different way, without scaling down the digital residual difference, or replacing the sinc filter with different components. Alternatively, the proposed algorithm is applied to other stages of the pipeline (even to all of them, with the exception of the last stage).

Naturally, in order to satisfy local and specific requirements, a person skilled in the art may apply to the solution described above many modifications and alterations all of which, however, are included within the scope of protection of the invention as defined by the following claims.

CLAIMS

1. An analog-to-digital converter (200) with a pipeline architecture for converting an analog input signal into a digital output signal with a predefined resolution, wherein the converter includes a plurality of stages (105_3-105_0) each one having means (110,115) for converting an analog local signal into a digital local signal with a local resolution lower than said resolution, means (120,125) for determining an analog residue indicative of a quantization error of the means for converting, and means (130) for amplifying the analog residue by an inter-stage gain corresponding to the local resolution to generate the analog local signal for a next stage, and wherein the converter further includes means (204) for combining the digital local signals of all the stages into the digital output signal weighting each digital local signal according to a digital weight depending on the corresponding inter-stage gain,

characterized in that

the means for combining includes, for at least one of the stages (105_3), means (205-240) for dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain, and means (230) for controlling the digital weight according to the digital correction signal.

2. The converter (200) according to claim 1, wherein the means (205-240) for estimating includes means (205-215) for inputting a digital test signal into the at least one stage and means (220-240) for deriving the digital correction signal from the digital test signal and the digital local signals of the next stages.

3. The converter (200) according to claim 2, wherein the digital test signal and the analog input signal are non-correlated, the means for deriving the digital correction signal including means (220-240) for correlating the digital test signal with the digital local signals of the next stages.

4. The converter (200) according to claim 3, wherein the digital test signal is pseudo-random.

5. The converter (200) according to claim 4, wherein the means (205-215) for inputting the digital test signal includes a pseudo-random generator (205) for generating the digital test signal, means (210) for converting the digital test signal into a corresponding analog test signal, and means (215) for adding the analog test signal to the analog local signal.

6. The converter (200) according to claim 5, wherein the means (220-240) for correlating includes means (220) for calculating a first digital signal multiplying the digital local signal by the digital weight, means (225,230) for calculating a second digital signal multiplying the digital local signal by the digital weight and the digital correction signal, means (235) for calculating the digital output signal summing the first digital signal, the second digital signal and the digital local signals of the next stages, and means (240) for calculating the digital correction signal from the digital test signal and the digital output signal.

7. The converter (200) according to claim 5 or 6, wherein the means (240) for calculating the digital correction signal includes means (305,310) for calculating a digital residual difference approximating a correlation

between the digital test signal and the digital output signal, means (315,320) for scaling down the digital residual difference, and an integrator (325,330) for converging towards the digital correction signal according to the digital residual difference.

8. The converter (200) according to claim 7, wherein the means (305,310) for calculating the digital residual difference includes a multiplier (305) for calculating a third digital signal multiplying the digital test signal by the digital output signal and a digital filter (310) for calculating the digital residual difference from the third digital signal.

9. The converter (200) according to any claim from 1 to 8, wherein the at least one stage consists of a sub-set of consecutive stages starting from a first stage.

10. A method of converting an analog input signal into a digital output signal with a predefined resolution using an analog-to-digital converter with a pipeline architecture including a plurality of stages, wherein for each stage the method includes the steps of:

converting an analog local signal into a digital local signal with a local resolution lower than said resolution,

determining an analog residue indicative of a quantization error of the means for converting, and

amplifying the analog residue by an inter-stage gain corresponding to the local resolution to generate the analog local signal for a next stage,

and wherein the method further includes the step of:

combining the digital local signals of all the stages into the digital output signal weighting each digital local signal according to a digital weight depending on the

corresponding inter-stage gain,

characterized in that

the step of combining includes, for at least one of the stages:

dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain, and

controlling the digital weight according to the digital correction signal.

ABSTRACT

A PIPELINE ANALOG-TO-DIGITAL CONVERTER WITH CORRECTION OF INTER-STAGE GAIN ERRORS

An analog-to-digital converter (200) with a pipeline architecture for converting an analog input signal into a digital output signal with a predefined resolution is proposed. The converter includes a plurality of stages (105_3-105_0) each one having means (110,115) for converting an analog local signal into a digital local signal with a local resolution lower than said resolution, means (120,125) for determining an analog residue indicative of a quantization error of the means for converting, and means (130) for amplifying the analog residue by an inter-stage gain corresponding to the local resolution to generate the analog local signal for a next stage, and further includes means (204) for combining the digital local signals of all the stages into the digital output signal weighting each digital local signal according to a digital weight depending on the corresponding inter-stage gain. In the converter of the invention, the means for combining includes, for at least one of the stages (105_3), means (205-240) for dynamically estimating a digital correction signal indicative of an analog error of the corresponding inter-stage gain, and means (230) for controlling the digital weight according to the digital correction signal.

(Figure 2)

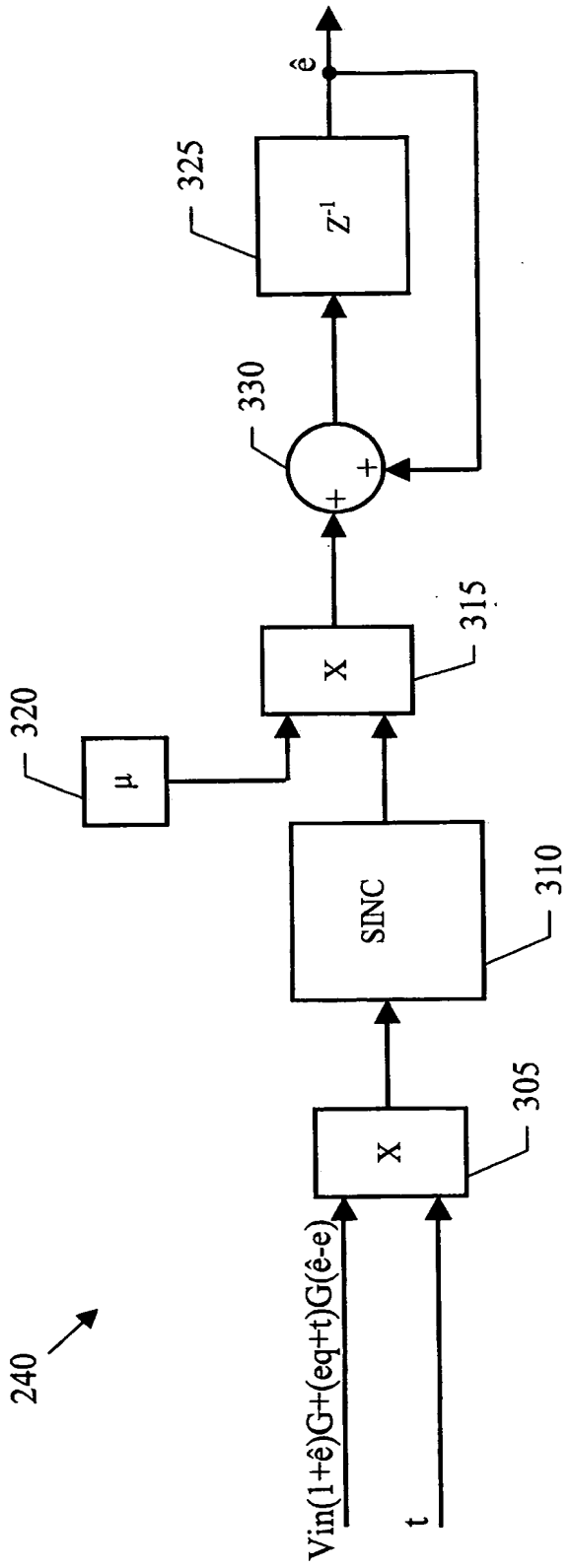

FIG.3

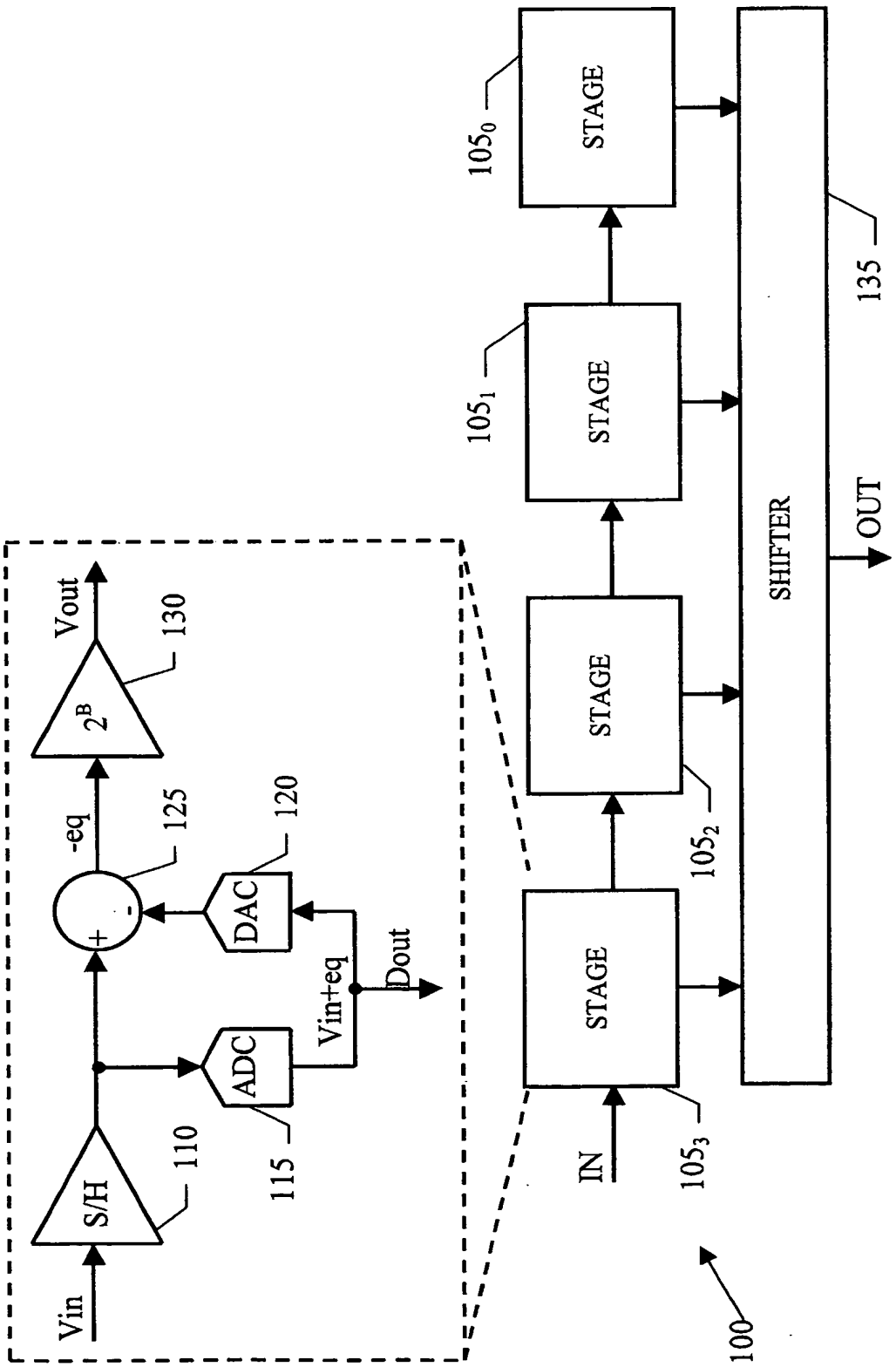
Vin
S/H
110
115
ADC
DAC
120
125
-eq
+
-
Vin+eq
Dout
Vout
2^B
130
IN
105_3
STAGE
105_2
STAGE
105_1
STAGE
105_0
STAGE
SHIFTER
135
OUT
100

FIG.1

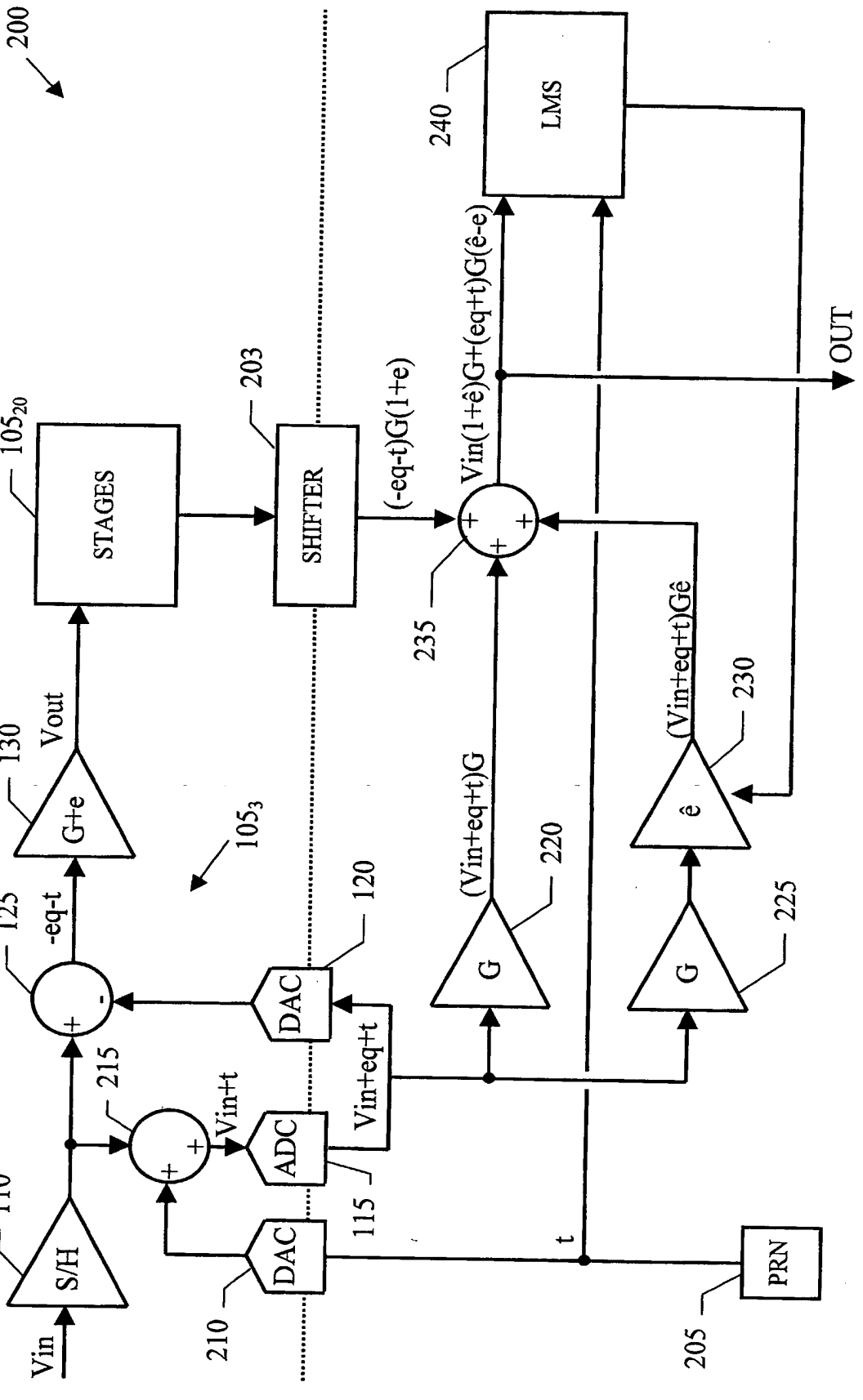
200
240
LMS
OUT
Vin(1+ê)G+(eq+t)G(ê-e)
203
105_{20}
STAGES
SHIFTER
(-eq-t)G(1+e)
235
130
Vout
G+e
105_3
125
-eq-t
120
DAC
(Vin+eq+t)G
220
G
(Vin+eq+t)Gê
230
ê
225
G
215
Vin+t
ADC
Vin+eq+t
115
110
S/H
DAC
210
t
205
PRN
Vin
204

FIG.2